CLAIMS

1. A method for forming an electronic device having a multilayer structure, comprising:

embossing a surface of a substrate so as to depress first and second regions of the substrate relative to at least a third region of the substrate;

depositing conductive or semiconductive material from solution onto the first and second regions of the substrate so as to form a first electrode on the first region and a second electrode on the second region, wherein the electrodes are electrically insulated from each other by the third region.

2. A method as claimed in claim 1, wherein the width of the third region is defined by the depth of embossing.

3. A method as claimed in claim 2, wherein the step of embossing is performed with a tool having an embossing surface, the embossing surface of the tool bearing at least one protruding portion having a sharp protruding tip wherein the width of the protruding portion widens from the sharp protruding tip, towards the embossing surface of the tool such that the width of a depressed region of the substrate, as measured in the plane of the surface of the substrate, is dependent on the depth of incursion of the at least one protruding edge of the tool into the substrate.

4. A method as claimed in claim 2, wherein the step of embossing is performed with a tool having an embossing surface, the embossing surface of the tool bearing at least one recessed portion having a recessed point wherein the width of the recessed portion widens from the recessed point, towards the embossing surface of the tool such that the width of a raised region of the substrate, as measured in the plane of the surface of the substrate, is dependent on the depth of incursion of the embossing surface of the tool into the substrate.

5. A method as claimed in any preceding claim, wherein after the step of embossing and prior to the step of depositing a solution of conductive or semiconductive material, the method further comprises the step of:

treating the surface of the substrate with a surface modification process that has a different effect on the depressed regions of the substrate relative to the non-depressed regions of the substrate whereby the raised regions and the depressed regions are given different surface energies, such that the deposition of the material is defined by the surface energy of the substrate in the first and second regions.

6. A method as claimed in any preceding claim, wherein the third region is a ridge wherein the width of the ridge defines a length of a channel of the electronic device.

7. A method as claimed in claim 6, wherein a cross section of the ridge is substantially rectangular.

8. A method as claimed in claim 6, wherein a cross section of the ridge is substantially triangular.

9. A method as claimed in claim any preceding claim, wherein the embossing step is performed at a temperature within 50 °C of the glass transition temperature of the topmost surface of the substrate.

10. A method as claimed in any of claims 1 to 5, wherein the embossing step is performed at a temperature at which the topmost surface of the substrate is in a liquid phase.

11. A method as claimed in any preceding claim, wherein the substrate comprises a flexible plastic substrate such as poly(ethleneterephtalate) (PET), polyethersulphone (PES) or polyethernaphtalene (PEN).

12. A method as claimed in any of claims 1 to 7, wherein the substrate comprises a rigid substrate coated with a polymer layer.

13. A method as claimed in claim 4, wherein said treating step comprises using a polymer layer with a high surface energy as the substrate.

14. A method as claimed in claim 4, wherein said treating step comprises exposing the substrate to one or more of an oxygen plasma, carbon-tetrafluoride plasma, ultra-violet or ozone surface treatment.

15. A method as claimed in claim 8, wherein said treating step comprises depositing a surface modifying layer onto the substrate at an oblique angle such that the surface modifying material is deposited onto the raised portions of the substrate, and the depressed portions are shadowed by the raised portions during the deposition of the surface modifying layer.

16. A method as claimed in claim 4, wherein said treating step comprises exposing the substrate to a physical etching method such as reactive ion etching.

17. A method as claimed in claim 4, wherein said treating step comprises applying a flat stamp to the surface.

18. A method as claimed in claim 17, wherein the flat stamp is inked with a self-assembled monolayer.

19. A method as claimed in claim 18, wherein the self-assembled monolayer is capable of bonding with functional groups on the surface of the substrate.

20. A method as claimed in claim 18 or 19, wherein the self-assembled monolayer is octyltrichlorosilane or fluoroalkyltrichlorosilane.

21. A method as claimed in claim 18, wherein the self-assembled monolayer comprises a methoxy silane.

22. A method as claimed in any preceding claim, wherein the solution of conductive or semiconductive material comprises a conductive ink.

23. A method as claimed in claim 22, wherein the conductive ink comprises a conductive polymer.

24. A method as claimed in claim 23, wherein the conductive polymer is polyethylenedioxythiophene doped with polystyrene sulfonic acid (PEDOT/PSS).

25. A method as claimed in claim 22, wherein the conductive ink comprises a conductive inorganic dispersion of electrically conductive nanoparticles.

26. A method as claimed in claim 22, wherein the conductive ink comprises a chemical precursor solution for an inorganic metal formulated in a solvent.

27. A method as claimed in any preceding claim, further comprising the step of depositing a layer of semiconductive material over the substrate and conductive or semiconductive material.

28. A method as claimed in claim 27, wherein said semiconductive material is regioregular poly(3-hexylthiophene) (P3HT) or poly(dioctylfluorene-co-bithiophene) (F8T2).

29. A method as claimed in claim 27, wherein said semiconductive material is an inorganic nanoparticulate or an inorganic nanowire semiconductor. .

30. A method as claimed in claim 27 to 29, further comprising the step of depositing a layer of dielectric over the layer of semiconductive material.

31. A method as claimed in claim 30, wherein the layer of dielectric comprises a polymer layer.

32. A method as claimed in claim 31, wherein the polymer layer is poly(methylmethracrylate) (PMMA).

33. A method as claimed in any of claims 29 to 32, further comprising the step of printing a pattern of conductive material to form an electrode for said electronic device.

34. A method as claimed in claim 33, wherein the electrode is formed from a conductive polymer or an inorganic material.

35. A method as claimed in any of claims 29 to 34, wherein both the semiconductor layer and the dielectric layer are patterned so as to form an active layer island of the device.

36. A method as claimed in any preceding claim, wherein the electronic device is a transistor.

37. A method as claimed in any preceding claim, wherein conductive material is deposited on the substrate which forms source and drain electrodes of the electronic device.

38. A method as claimed in any of claims 30 to 37, wherein the layer of dielectric deposited over the semiconductive layer is a gate dielectric layer.

39. A method as claimed in claim 38, further comprising the step of depositing a gate electrode onto the surface of the gate dielectric layer.

40. A method as claimed in any preceding claim, wherein the embossing step is performed with a tool having an embossing surface suitable for embossing the substrate, the embossing surface bearing an array of protruding features with sharp tips.

41. A method as claimed in claim 40, wherein the radius of curvature of the sharp edges is less than 100 μm.

42. A method as claimed in claim 40, wherein the radius of curvature of the sharp edges is less than 10 μm.

43. A method as claimed in claim 40, wherein the protruding features have a rectangular profile.

44. A method as claimed in any preceding claim, wherein the width of the third region is less than 20 μm.

45. A method as claimed in any preceding claim, wherein the width of the third region is less than 5 μm.

46. A method as claimed in any preceding claim, wherein the width of the third region is less than 1 μm.

47. A method as claimed in any preceding claim, wherein the substrate comprises a functional layer of the electronic device, wherein the functional layer comprises one of a conducting material and a semiconducting material.

48. A method for forming a transistor comprising:

depositing an electrically conductive layer onto a substrate;

embossing the substrate and the conductive layer such that a portion of the conductive layer is pushed into the substrate thereby forming a depressed region and electrically insulating the portion of the conducting layer in the depressed region from the remaining at least one region of the electrically conductive layer;

at least one portion of the conductive layer forming an electrode of the transistor.

49. A method as claimed in claim 48, wherein the portion of the electrically conductive layer in the depressed region and a portion of the conductive layer in the remaining region form source and drain electrodes of the transistor.

50. A method as claimed in claim 48, wherein the depressed region separates and electrically insulates at least two remaining regions of the conductive layer, wherein at least two regions form source and drain electrodes of the transistor.

51. A method as claimed in claim 48 or 50, wherein the electrically conductive layer in the depressed region forms a floating conducting bridge in a channel of the transistor.

52. A method as claimed in any of claims 48 to 51, wherein the method further comprises the step of depositing at least one additional non-planarizing layer on top of the embossed substrate, such that the topographic profile of each non-planarizing layer conforms to that of the substrate.

53. A method as claimed in claim 52, wherein the method further comprises the step of depositing at least one pattern of a material onto one of the non-planarizing layers.

54. A method as claimed in claim 53, wherein at least one pattern of a material is deposited onto a depressed region of the non-planarizing layer, the material dèposited such that the lateral location of the material is defined by the shape of the non-planarizing layer.

55. A method as claimed in claim 54, wherein the material deposited into the depressed region of the non-planarizing layer defines an active region of the transistor whereby the active region is laterally aligned with the topographic profile of the non-planarizing layer.

56. A method as claimed in any of claims 53 to 55, wherein the material is a conductive or semiconductive material.

57. A method as claimed in claim 56, wherein the pattern of a material comprises a gate electrode.

58. A method as claimed in any of claims 52 to 57, wherein the at least one additional non-planarizing layer comprises depositing a first non-planarizing layer and a second non-planarizing layer.

59. A method as claimed in claim 58, wherein said first non-planarizing layer is a semiconductor layer.

60. A method as claimed in claim 58 or 59, wherein said second non-planarizing layer is a dielectric layer.

61. A method as claimed in any of claims 48 to 60, wherein the substrate is a flexible electrically insulating substrate.

62. A method as claimed in claim 61, wherein the flexible electrically insulating substrate is one of poly(ethleneterephtalate) (PET), polyethersulphone (PES) or polyethernaphtalene (PEN).

63. A method as claimed in any of claims 48 to 60, wherein the substrate is a rigid substrate containing at least one flexible polymer layer that is electrically insulating.

64. A method as claimed in any of claims 53 to 63, further comprising the step of, prior to the deposition of at least one pattern of a material, performing a surface modification process on the non-planarizing layer that has a different effect on relatively raised regions of the non-planarizing layer in comparison to relatively depressed regions of the non-planarizing layer, so as to generate a surface energy contrast between the relatively raised and relatively depressed regions of the non-planarizing layer in order to confine the deposition of the at least one pattern of a material to the depressed region.

65. A method as claimed in claim 64, wherein the surface modification process comprises using a flat stamp to deposit a surface energy barrier in the raised regions of the non-planarizing layer.

66. A method as claimed in any of claims 48 to 65, wherein one or both of the sides along the length of the boundary between the depressed region and the raised region is non linear in the plane of the substrate.

67. A method as claimed in claim 48, wherein a layer of semiconducting material is deposited onto the substrate prior to the step of depositing the layer of conductive material onto the substrate.

68. A method as claimed in claim 48, wherein the substrate comprises a layer of semiconducting material that forms part of the active layer of the transistor.

69. A method as claimed in claim 68, further comprising the steps of:

coating the embossed structure with a non-planarizing layer of gate dielectric; and

depositing a gate electrode onto the layer of gate dielectric layer, such that the gate electrode is aligned with the embossed region of the substrate.

70. A method as claimed in claim 69, wherein the gate electrode is confined by a surface energy barrier to a depressed region of the gate dielectric conformal to the depressed region of the substrate.

71. A method for solution deposition of at least one pattern of material on a substrate comprising the steps of:

depositing one or more polymer layers onto a surface of the substrate;

embossing the one or more polymer layers so as to define at least one depressed region and at least one raised region;

etching the one or more polymer layers so as to reveal the surface of the substrate in the areas defined by the one or more depressed regions of the

embossing step, and leaving a mask layer of polymer layer material in the areas defined by the one or more raised regions; and

depositing a layer of material on to the substrate surface from solution, such that the deposition is confined by the area defined by the mask.

72. A method as claimed in claim 71, wherein said at least one pattern of material is at least one conducting electrode.

73. A method as claimed in claim 71, wherein said at least one pattern of material comprises a semiconductor or a dielectric.

74. A method as claimed in any of claims 71 to 73, wherein the mask layer of polymer material left on the substrate after the etching step has a different surface energy to the substrate.

75. A method as claimed in any of claims 71 to 74, wherein the substrate is a hydrophilic substrate.

76. A method as claimed in any of claims 71 to 75, wherein the substrate comprises a flexible plastic substrate such as poly(ethleneterephtalate) (PET), polyethersulphone (PES) or polyethernaphtalene (PEN).

77. A method as claimed in claim 75, wherein the step of depositing one or more polymer layers comprises:

depositing a hydrophobic polymer layer onto the substrate;

subsequently depositing a sacrificial polymer layer; and

removing the sacrificial polymer layer.

78. A method as claimed in claim 77 wherein the hydrophobic polymer layer is a layer of polyimide.

79. A method as claimed in claim 77 wherein the hydrophobic polymer layer has an aligned molecular structure.

80. A method as claimed in claim 78 wherein the aligned molecular structure of the hydrophobic polymer layer is imposed by mechanical rubbing.

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81. A method as claimed in claim 78 wherein the aligned molecular structure of the hydrophobic polymer layer is imposed by exposure to linearly polarised light.

82. A method as claimed in claim 77 wherein the sacrificial polymer layer comprises polyvinylphenol.

83. A method as claimed in claim 77 wherein the sacrificial polymer layer comprises novolak.

84. A method as claimed in claim 77 wherein the sacrificial polymer layer comprises polymethylmethracrylate (PMMA).

85. A method as claimed in claim 71 further comprising the steps of:

modifying the surface energy of the substrate in the regions left exposed by the mask layer;

removing the mask layer of polymer material in a second etching step, which has substantially no further effect on the surface energy of the substrate, so as to leave a surface energy pattern on the surface of the substrate conformal to the initial embossing, prior to the step of depositing a layer of material on to the substrate surface.

86. A method as described in claim 85, wherein the step of modifying the surface energy of the surface layer comprises exposing the surface layer to a vapour of a self-assembling monolayer.

87. A method as described in claim 85, wherein the step of modifying the surface energy of the surface layer comprises exposing the surface layer to an oxygen plasma or ultra violet / ozone surface treatment.

88. A method as claimed in claim 85, wherein the step of modifying the surface energy of the surface layer comprises exposing the surface layer to a carbon tetrafluoride plasma treatment.

89. A method as claimed in claim 85, wherein the step of removing the mask layer such that the surface energy of the modified regions is unchanged comprises washing in a solvent in which the mask layer is soluble, but the surface layer is insoluble.

90. A method as claimed in any of claims 71 to 89 wherein the one or more polymer layers is a planarizing layer deposited by spin coating.

91. A method as claimed in claim 90, wherein the planarizing layer is a polymer deposited from solution.

92. A method as claimed in any of claims 71 to 91, wherein the etching step comprises oxygen plasma etching.

93. A method as claimed in claim 85, wherein said step of modifying the surface energy comprises depositing a surface modifying layer onto the substrate at an oblique angle such that the surface modifying material is deposited onto the

raised portions of the substrate, and the depressed portions are shadowed by the raised portions during the deposition of the surface modifying layer.

94. A method as claimed in any of claims 71 to 93, wherein said etching step comprises exposing the substrate to a physical etching method such as reactive ion etching.

95. A method as claimed in any of claims 71 to 94 wherein the embossing step comprises pressing an embossing tool containing an array of protruding features into the substrate.

96. A method as claimed in claim 86, wherein the self-assembling monolayer is capable of reacting with a functional group present on the substrate surface.

97. A method as claimed in claim 96 further comprising the step of treating the surface of the substrate so as to increase the number of functional groups on the surface of the substrate.

98. A method for forming an electronic device comprising the steps of:

depositing one or more polymer layers onto a surface of the substrate;

embossing the one or more polymer layers so as to define at least one depressed region and at least one raised region;

etching the one or more polymer layers so as to reveal the surface of the substrate in the areas defined by the one or more depressed regions of the embossing step, and leaving a mask layer of polymer layer material in the areas defined by the one or more raised regions; and

depositing a layer of material on to the substrate surface from solution, such that the deposition is confined by the area defined by the mask.

99. A method for forming an electrode of a multi-layer electronic device having an active channel region defined between at least two layers of the device, the method comprising:

defining a topographic feature on a surface of a first layer of the device; and

depositing a layer of a conductive material onto the topographic feature for forming an electrode;

wherein one of the relatively raised and relatively lowered regions of the conductive material interacts during operation of the electronic device with another layer of the device to which it is closer than the other of the relatively raised and relatively lowered regions to define an active channel of the device.

100. A method as claimed in claim 99, wherein the step of defining a topographic feature on a surface comprises a step of embossing the surface.

101. A method as claimed in claim 99 or 100, wherein the first layer of the device is a dielectric.

102. A method as claimed in claim 100, wherein the method further comprises, prior to the step of embossing:

defining a source and a drain electrode on a substrate such that the area between the source and drain electrodes forms the active channel region of the electronic device;

depositing a layer of semiconductor over the electrodes;

depositing a layer of dielectric over the layer of semiconductor forming the first layer of the device, the exposed surface of which is the surface that is embossed.

103. A method as claimed in any of claims 99 to 102, wherein the electrode formed is a gate electrode.

104. A method as claimed in any of claims 80 to 103, wherein the active channel region of an electronic device is an active channel region of a transistor.

105. A method as claimed in claim 99, wherein the electrode of a multi-layer electronic device is a gate electrode of a top-gate transistor wherein the active channel region is defined by an area between a source and a drain electrode deposited on a substrate, the method further comprising the steps of:

depositing a layer of semiconductor over the electrodes;

depositing a layer of dielectric over the layer of semiconductor forming the first layer of the device;

wherein the step of defining a topographic feature on a surface of the first layer of the device comprises embossing the dielectric layer;

whereby the relatively lowered region of the conductive material interacts with the active channel region of the device more strongly than the relatively raised region of the conductive material interacts with the active channel region of the device.

106. A method as claimed in claim 101, wherein the method further comprises the step of embossing a second region of the dielectric layer in the region of a pixel electrode.

107. A method as claimed in claim 106, wherein the pixel electrode is connected to one of the source and drain electrodes of the electronic device.

108. A method as claimed in claim 106 or 107, wherein a second electrode is deposited in the second embossed region of the dielectric so as to form a pixel capacitor.

109. A method as claimed in claim 99, wherein the first layer on which the topographic feature is defined is a substrate.

110. A method as claimed in any of claims 99 to 109, wherein the substrate comprises a flexible plastic substrate such as poly(ethleneterephtalate) (PET), polyethersulphone (PES) or polyethernaphtalene (PEN).

111. A method as claimed in claim 109, wherein the topographic feature is defined on the substrate by at least one of the following:

direct-write deposition;

lithographic patterning; and

embossing.

112. A method as claimed in claim 111, wherein the layer of conductive material is conformal.

113. A method as claimed in claim 111 or 112, wherein the multi-layer electronic device is a bottom-gate transistor and the layer of conductive material deposited on the topographic feature is conformal, the method further comprising the steps of:

depositing a planarizing layer of dielectric over the electrode;

depositing a source and a drain electrode on the surface of the dielectric; and

depositing a layer of semiconductor over the source and drain electrodes.

114. A method as claimed in claim 113, wherein a surface energy pattern is defined on the surface of the dielectric prior to the deposition of the source and the drain electrode.

115. A method as claimed in claim 113, wherein the step of depositing a planarizing layer of dielectric comprises at least one of:

a spin-coating step;

a blade coating step;

a spray coating step; and

a slot coating step.

116. A method as claimed in claim 99 or 100, wherein the electrode of a multi-layer electronic device is a gate electrode of a bottom-gate transistor and wherein the first layer of the device is a substrate, the method further comprising the steps of:

depositing a planarizing layer of dielectric over the electrode;

depositing a source and a drain electrode on the surface of the dielectric wherein the active channel region is defined by an area between the source and the drain electrodes;

depositing a layer of semiconductor over the source and drain electrodes;

whereby the relatively raised region of the conductive material interacts with the active channel region of the device more strongly than the relatively lowered region of the conductive material interacts with the active channel region of the device.

117. A multi-layer electronic device having an active channel region defined between at least two layers of the device, the device comprising:

a topographic feature on a surface of a first layer of the device; and

an electrode formed by a layer of a conductive material deposited on the topographic feature;

wherein during operation of the electronic device, one of the relatively raised and relatively lowered regions of the conductive material interacts with

another layer of the device to which it is closer than the other of the relatively raised and relatively lowered regions to define an active channel of the device.

118. A device as claimed in claim 117, wherein the first layer of the device is a gate dielectric layer.

119. A device as claimed in claim 118, wherein the thickness of the gate dielectric layer is relatively smaller in the active channel region of the device.

120. A device as claimed in claim 117, wherein the electrode formed is a gate electrode.

121. A device as claimed in claim 117 or 120, wherein the first layer of the device is a substrate.

122. A device as claimed in any of claims 117, 120 or 121, further comprising a planarizing gate dielectric layer deposited over the first layer and the electrode.